In the Claims

This listing of claims will replace all prior versions, and listings, of claims.

Listing of Claims

1. (currently amended): A method of forming a dual damascene interconnect in an integrated circuit comprising:

providing a substrate having a first etched region therein;

filling said first etched region with a protective layer;

coating said protective layer with a resist layer;

successively patterning said resist layer and said protective layer to define an opening encompassing said first etched opening wherein said protective layer is recessed within said first etched opening;

thereafter forming a second etched region encompassing a top portion of said first etched region;

thereafter removing said resist layer and said protective layer; and

thereafter filling said first and second etched regions with a conductive material to complete formation of said interconnect.

2. (Original): The method according to claim 1 wherein said protective material is a bottom antireflective coating (BARC) material.

3. (Original): The method according to claim 2 wherein said BARC material has the following properties: it absorbs light at a wavelength used to expose said resist; it completely fills said first etched region; and it can be partially removed by a developer used to remove said resist.

4. (Original): The method according to claim 2 wherein said BARC material comprises polyimide or organic type ARC material.

5. (Original): The method according to claim 1 wherein said first etched region forms a via hole and wherein said second etched region forms a trench and wherein said via hole and said trench together form a dual damascene opening.

6. (Original): The method according to claim 1 wherein the said protective layer recessed within said first etched region has a height of between about 50% and 95% of a height of said first etched region.

7. (Original): The method according to claim 1 wherein said first and second etched region are etched through an insulating layer comprising silicon dioxide or low dielectric constant dielectric materials.

8. (Original): The method according to claim 7 further comprising depositing a hard mask layer overlying said insulating layer prior to forming said first etched region wherein said hard mask layer comprises silicon nitride.

9. (currently amended): A method of forming a dual damascene interconnect in an integrated circuit comprising:

providing a substrate having a first etched region therein;

filling said first etched region with a bottom antireflective coating (BARC) layer;

coating said BARC layer with a resist layer;

successively patterning said resist layer and said BARC layer to define an opening encompassing said first etched opening wherein said BARC layer is recessed within said first etched opening;

thereafter forming a second etched region encompassing a top portion of said first etched region;

thereafter removing said resist layer and said BARC layer; and

thereafter filling said first and second etched regions with a conductive material to complete formation of said interconnect.

10. (Original): The method according to claim 9 wherein said BARC material has the following properties: it absorbs light at a wavelength used to expose said resist; it completely fills said first etched region; and it can be partially removed by a developer used to remove said resist.

11. (Original): The method according to claim 9 wherein said BARC material comprises polyimide or organic type ARC material.

12. (Original): The method according to claim 9 wherein said first etched region forms a via hole and wherein said second etched region forms a trench and wherein said via hole and said trench together form a dual damascene opening.

13. (Original): The method according to claim 9 wherein the said BARC layer recessed within said first etched region has a height of between about 50% and 95% of a height of said first etched region.

14. (Original): The method according to claim 9 wherein said first and second etched region are etched through an insulating layer comprising silicon dioxide or low dielectric constant dielectric materials.

15. (Original): The method according to claim 14 further comprising depositing a hard mask layer overlying said insulating layer prior to forming said first etched region wherein said hard mask layer comprises silicon nitride.

16. - 23. (Canceled).